ABSTRACT

Methods and apparatus are disclosed for erasing a core memory cell using a negative gate voltage in a semiconductor memory device, wherein negative pump MOS regulation capacitors are pre-charged according to a pre-charge signal during a core cell erase operation. A negative voltage pump is then regulated using the pre-charged negative pump MOS regulation capacitors to provide the negative gate voltage. Apparatus is disclosed for pre-charging negative pump MOS regulation capacitors during a core cell erase operation in a memory device, which comprises a switch connected between a reference voltage and the negative pump MOS regulation capacitors, and a pre-charge control circuit providing a pre-charge signal to the switch to selectively connect the reference voltage to the negative pump MOS regulation capacitors for pre-charging thereof in an erase operation.